A diagram of a computer

Description automatically generated

A white board with writing on it

Description automatically generated

64 bit processor

16 registers (4 bits)

5 bits for instructions (32 instructions)

4 cores goal to be able to run multiple processes at once

Memory – maybe change number of addresses to match with imm size for imm type so can reference specific word from an imm instruction

61 addresses 3 selection bits for 8 8bit words per address

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Memory Address | Wordlet 7 | Wordlet 6 | Wordlet 5 | Wordlet 4 | Wordlet 3 | Wordlet 2 | Wordlet 1 | Wordlet 0 |
| 0x000000…000 | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] |
| 0x000000…001 | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] |
| 0x000000…002 | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] | [8 bits] |

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| --- | --- | --- | --- | --- |
| Instruction | Name | Type | Opcode | Description |
| SLL | Shift left logical |  |  |  |
| SLLI | Shift left logical immediate |  |  |  |
| SRL | Shift right logical |  |  |  |
| SRLI | Shift right logical immediate |  |  |  |
| SWL | Store wordlet |  |  |  |
| SW | Store word |  |  |  |
| SHW | Store half word |  |  |  |
| LWL | Load wordlet |  |  |  |
| LW | Load word |  |  |  |
| LHW | Load halfword |  |  |  |
| ADD | Add |  |  |  |
| ADDI | Add imm |  |  |  |
| SUB | Subtract |  |  |  |
| SUBI | Subtract imm |  |  |  |
| XOR |  |  |  |  |
| XORI |  |  |  |  |
| OR |  |  |  |  |
| ORI |  |  |  |  |
| AND |  |  |  |  |
| ANDI |  |  |  |  |
| BEQ |  |  |  |  |
| BNE |  |  |  |  |
| BGE |  |  |  |  |
| BLT |  |  |  |  |
| BLTU | Branch less than unsigned |  |  |  |
| BGEU | Branch greater equal unsigned |  |  |  |
| JAL |  |  |  |  |
| JALR |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
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